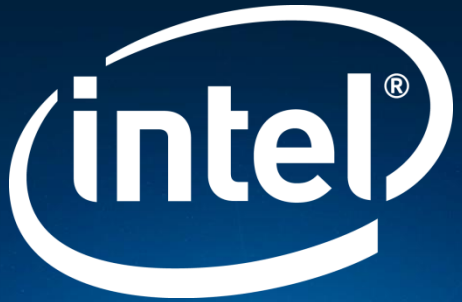
FRANK FERRANTE

October 2019



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Heterogeneous 3D System-in-Package (SiP) Integration

Efficient and scalable integration using Intel's Embedded Multi-Die Interconnect Bridge (EMIB)

New class of FPGAs and MCPs to enable higher efficiency and flexibility

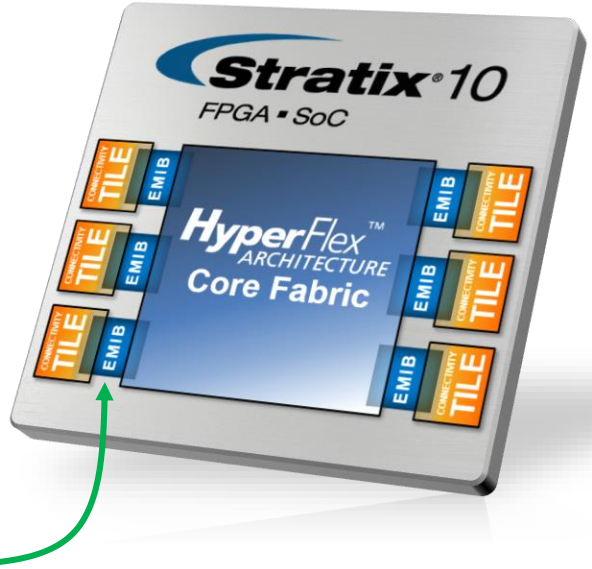
Enables convergence of process nodes and system functions into a single device

- Mix and match process nodes

Enables higher efficiency and flexibility

- Up to 1 Tbps full duplex on each EMIB Interface

Reduces size, weight and power



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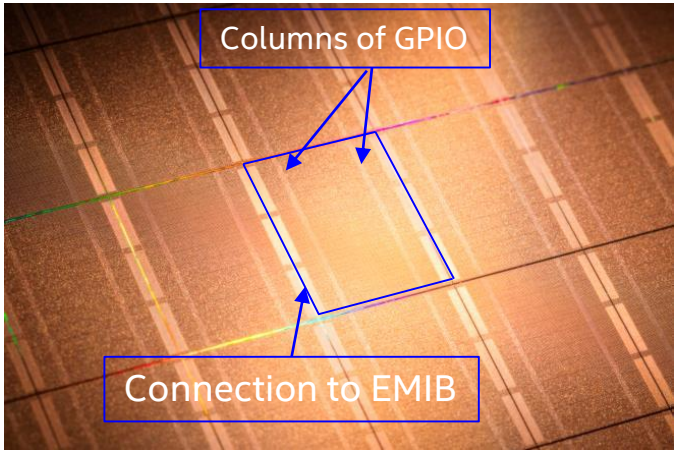
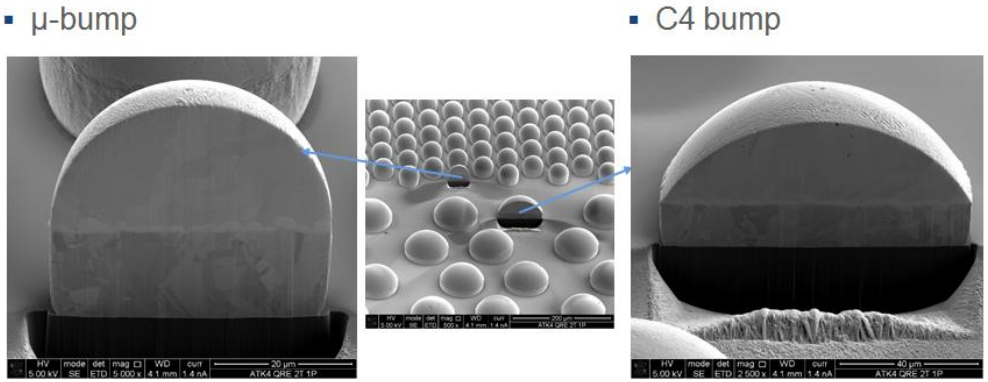
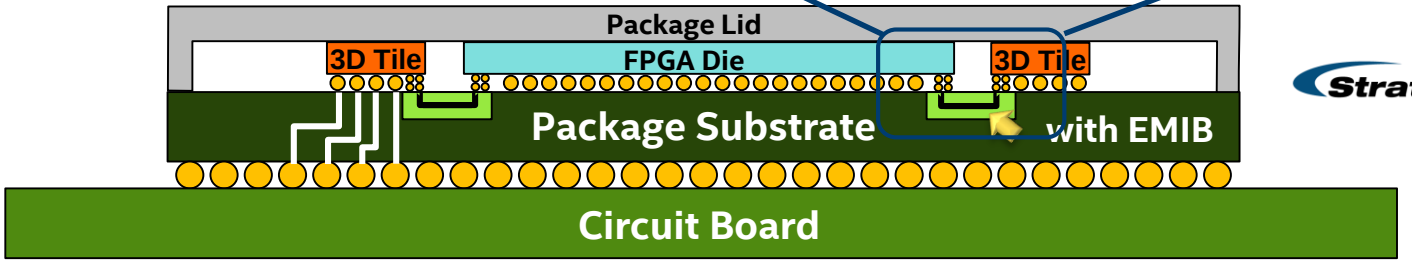


EMIB - Intel's **E**mbedded **M**ulti-Die **I**nterconnect **B**ridge

Bump Images



Stratix 10 Packaging with EMIB Technology



Stratix 10

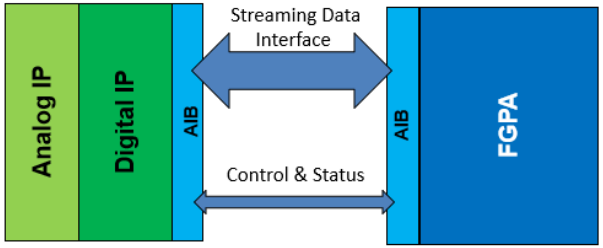
AIB Overview

Supports peer-to-peer high bandwidth parallel communication

Versatile per-channel clocking in both directions

Streaming or transactional protocols can be implemented on top of AIB

AIB's flexible IO cell permits arbitrary TX, RX, clock and control mapped by the protocol layer above



AIB Power Advantages

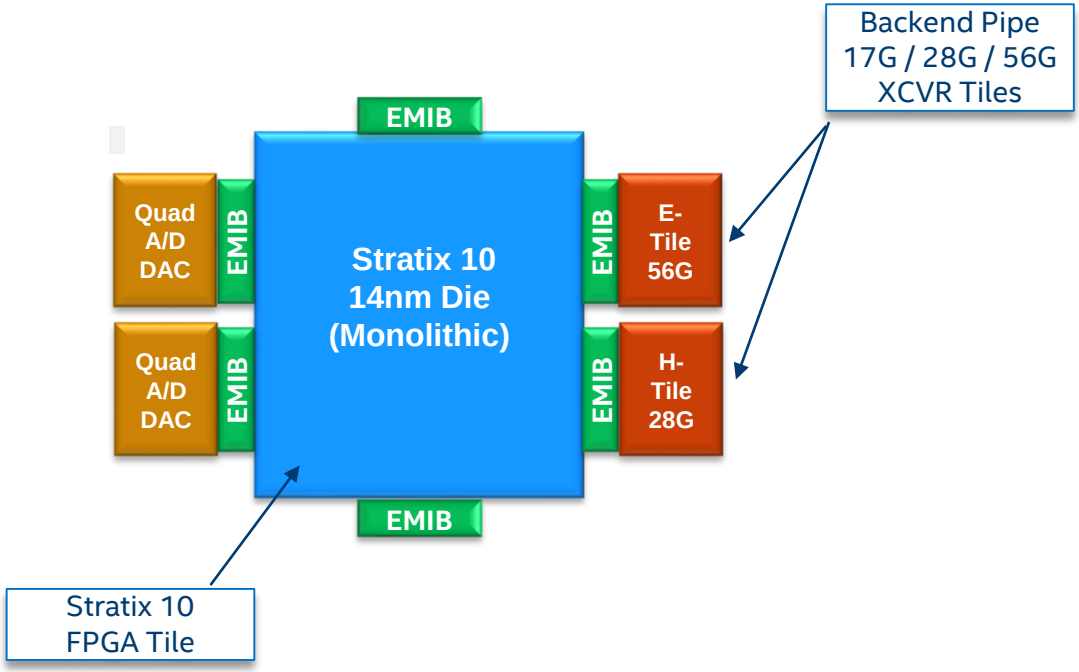
Metric	SERDES	AIB
Energy	17pJ/bit [12]	1 pJ/bit [11]
Power (500Gbps example)	8.5W	0.5W

AIB Latency Comparisons

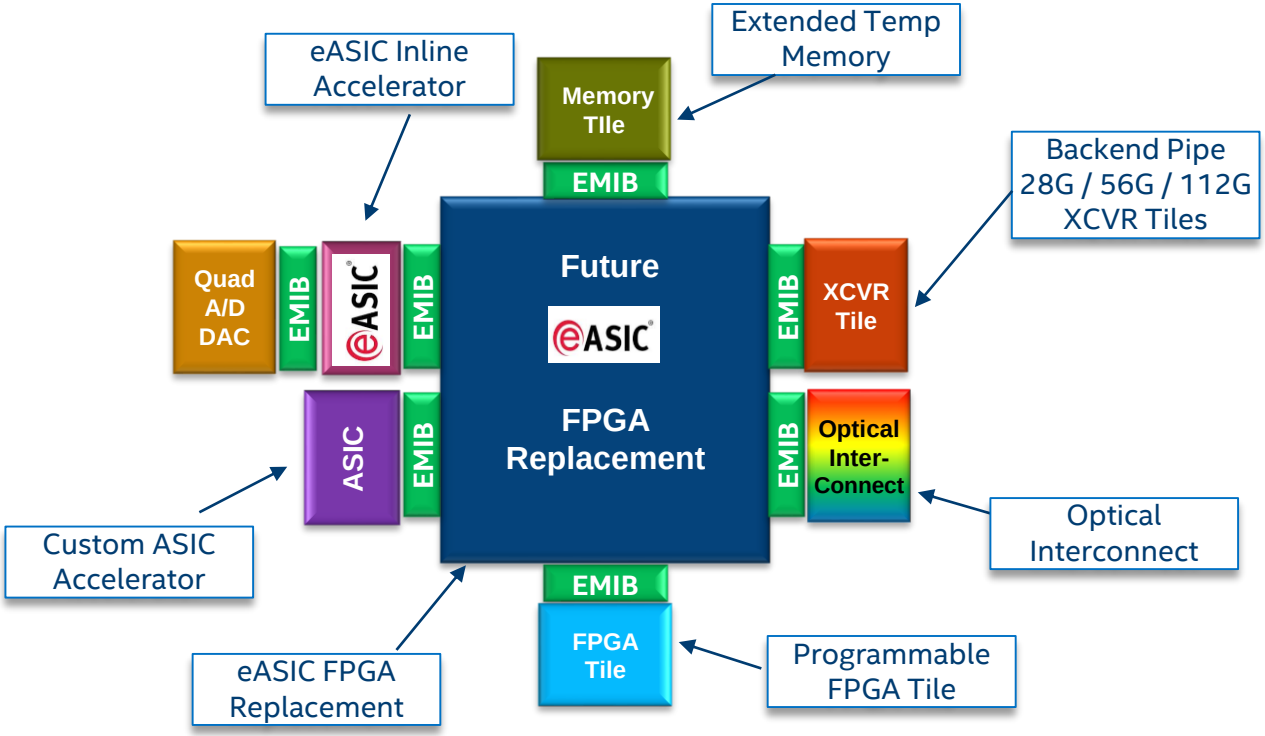
	JESD204C	AIB	
Maximum line rate	*32*	*2*	*Gbps*
Total Digital Delay TX	17.53	0.75	ns
Analog Delay TX	2	1	ns
PCB/interposer Delay	0.31	0.06	ns
Analog Delay RX	2	1	ns
Total Digital Delay RX	20.62	0.75	ns
Total Delay	**42.46**	**3.56**	**ns**

The performance figures shown are optimized on Intel technology. Performance varies based upon system configuration.

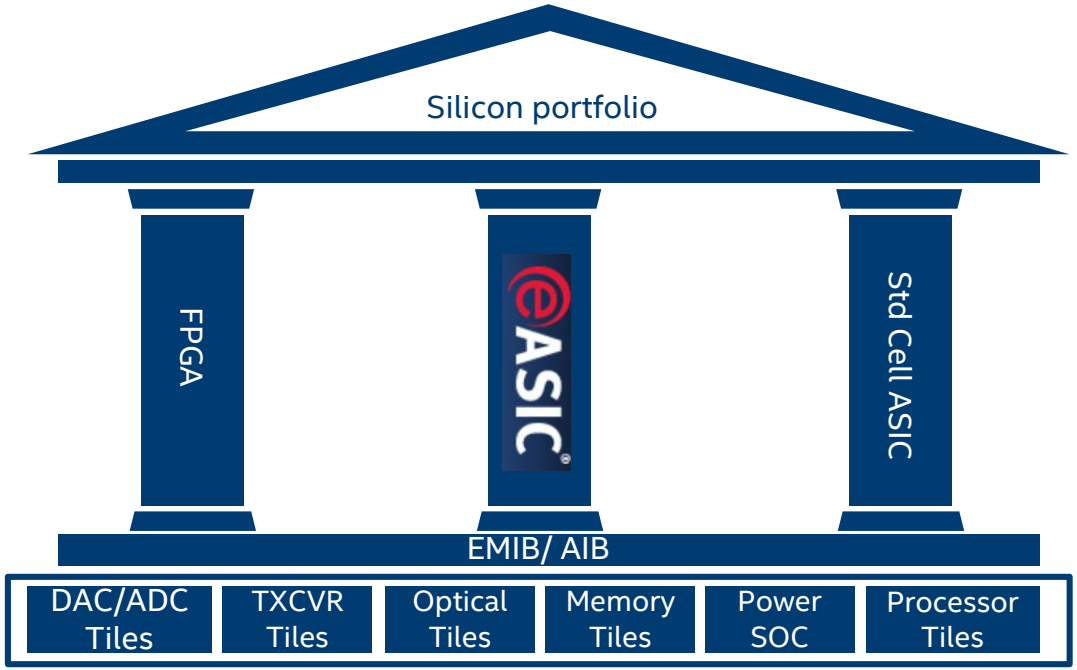
Integrated Mixed Signal 2



Future System Concept: + Customer ASIC



Scalable Platform Strategy



Enable silicon programmability and hardened customization

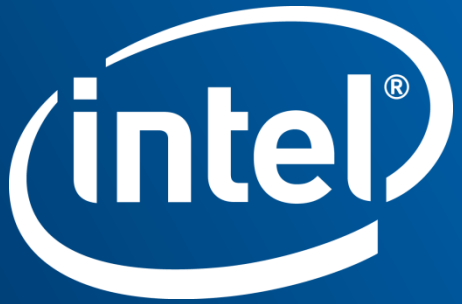
- ✓ Optimized by market
- ✓ Further optimized by customer
- ✓ Tailored capability to desired combination of TTM, cost, power, integration

Reduce customer's R&D spend

- ✓ Consistent IP across pillars
- ✓ Software and package compatibility
- ✓ Maximizes reuse

Mix and match pillars and tiles

- ✓ Leverage chiplet strategy to integrate independent of node
- ✓ Blend pillar components for optimal power, performance, cost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